What is claimed is:

1. A decoder circuit in a flash memory device comprising;

a global row decoder for outputting a global word line signal, said global row decoder consisted of a first decoding means selected according to a row address signal and a second decoding means to which an output signal of said first decoding means and an erasure signal are input; and

a local row decoder for selecting each global word line signal outputted from the said global row decoder.

2. The decoder circuit of claim 1, wherein said first and second decoding means are consisted of NAND gates.

3. The decoder circuit of claim 1, wherein said local row decoder is consisted of;

a first and second transistors to said word line signal is input;

and a third, fourth and fifth transistors outputting a first voltage supply signal and a second voltage supply signal to a sector word line.

4. The decoder circuit claim 3, wherein said second, third and fourth transistors are consisted of PMOS transistor, and said first and fifth transistors are consisted of NMOS transistor.

5. A decoder circuit in a flash memory device, comprising:

a global row decoder for outputting a global word line signal; and

a local row decoder for selecting a word line in response to said global word line signal of said global row decoder.

6. The decoder circuit of claim 5, wherein said global row decoder is consisted of;

a first and second transistors to which XnCOM signal is input, and

a third and fourth transistors, to which an output voltage of said ~~frist~~ first and second transistors, is input for outputting a Vppx or Veex to a global sector word line.

7. The decoder circuit claim 6, wherein said first and third transistors are consisted of PMOS transistor, and said second and fifth transistors are consisted of NMOS transistor.

8. The decoder circuit of claim 5, wherein said local row decoder is consisted of a fifth, sixth and seventh transistor, to which said global word line is input, ~~frist~~ first and second transistors, for outputting said global word line to said word line.

9. The decoder circuit claim 8, wherein said fifth transistor is consisted of

PMOS transistor, and said sixth and seventh transistors are consisted of NMOS transistor.